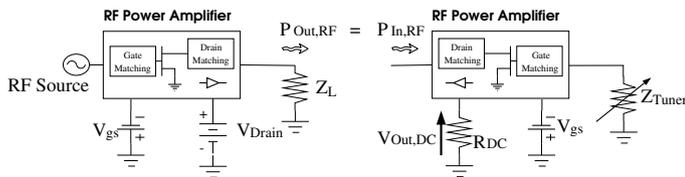


# Time-reversal duality of high-efficiency RF power amplifiers

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This paper discusses the similarity between RF power amplifiers and rectifiers. We show that the same high-efficiency harmonically-terminated power amplifier can be operated in a dual rectifier mode. Nonlinear simulations with a GaN HEMT transistor model show the time-reversal intrinsic voltage and current waveform relationship between a class-F amplifier and rectifier. Measurements on a class-F<sup>-1</sup> amplifier and rectifier at 2.14 GHz demonstrate over 80% efficiency in both cases.

**Introduction:** High-efficiency RF power amplifiers are designed by presenting appropriate output impedances at the fundamental and harmonic frequencies, in order to shape the current and voltage waveforms across the current source of the device in a way that minimizes the power dissipation  $v(t) \cdot i(t)$ . In the past few years, PAs implemented in GaN HEMT technologies have demonstrated power added efficiencies (PAEs) above 80% using a single transistor. In this letter, we show that a harmonically-terminated transistor amplifier is a bidirectional device that exhibits high efficiency in both amplifier and rectifier modes. High power conversion efficiency of a power amplifier (DC to RF) and a rectifier obtained by operating the amplifier in reverse (RF to DC) is achieved with time-reversal duality [1] of the transistor's main current source. In other words, the power amplifier (PA) and rectifier (R) drain terminal voltage and current are related by  $v_{PA}(t) = v_R(t)$  and  $i_{PA}(t) = -i_R(t)$ , respectively. The block diagram in Fig. 1 shows the main PA and rectifier parameters that are discussed here.



**Fig. 1** Block diagram of a power amplifier circuit operated in PA mode (left) and rectifier mode (right).

In the remainder of the letter, simulations of a class-F amplifier based on a GaN HEMT are used to illustrate the time-reversal duality of power amplifiers and rectifiers. This example uses a nonlinear device model in a high-efficiency amplifier circuit. Non-linear simulations result in time-reversed dual current and voltage waveforms at the virtual drain of the PA and rectifier. After the principle is demonstrated through simulations of intrinsic waveforms, measurements on a class-F<sup>-1</sup> GaN power amplifier using a TriQuint device are compared for PA and rectifier configurations, with the goal of demonstrating that this duality holds for various high-efficiency amplifier and rectifier circuits.

**Simulations of PA and rectifier:** Simulations have been performed with the 8x75 μm GaN HEMT model described in [2] at 2.14 GHz. This non-linear model includes: non-linear capacitances C<sub>gs</sub>, C<sub>gd</sub> and C<sub>ds</sub>; gate-source and gate-drain diodes; and breakdown and trapping effects. This model reproduces the nonlinear transistor behavior not only for positive, but also for negative values of the drain voltage.

For the amplifier mode of operation, when an input RF signal is injected into the gate terminal, we consider the drain efficiency, or DC-to-RF conversion efficiency:

$$\eta_{PA} = \frac{P_{out,RF}}{P_{DC}} \quad (1)$$

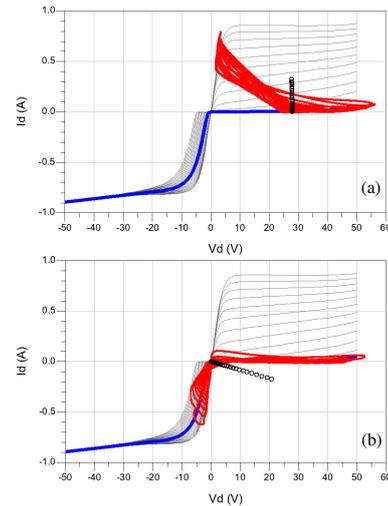
In class-F mode with 5 harmonics terminated, for V<sub>ds</sub> = 28V and V<sub>gs</sub> = -4.9V, an amplifier efficiency  $\eta_{PA} = 72\%$  is obtained. The simulated behavior of the transistor is depicted on Fig. 2 (a) and 3 (a), showing the I-V curves and load-line, and intrinsic drain voltage and current waveforms, respectively.

The same class-F PA circuit is next simulated in rectifier mode, where the drain DC power supply is replaced by a DC load R<sub>DC</sub>. The input to the circuit is now RF power P<sub>in,RF</sub> equal to P<sub>out,RF</sub> of the amplifier,

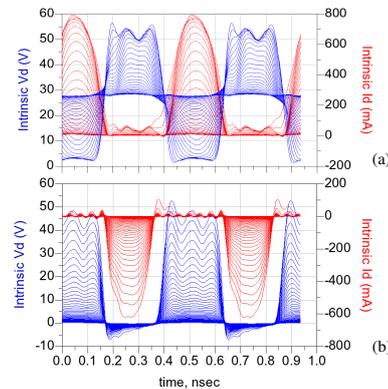
and injected at the drain port as illustrated on Fig. 4. Assuming the DC gate current is negligible, the rectifier RF-to-DC conversion efficiency is

$$\eta_R = \frac{P_{DC}}{P_{in,RF}} = \frac{2|V_{DC}|^2}{R_{DC} \Re\{V_{drain}(f_0)I_{drain}^*(f_0)\}} \quad (2)$$

An impedance tuner connected at the gate input of the PA allows load-pull at the gate resulting in  $\eta_R = 80\%$  with R<sub>DC</sub> = 120Ω (f<sub>RF</sub> = 2.14GHz). Fig. 2 (b) and 3 (b) illustrate the behavior of the transistor for RF gate load impedance that maximizes rectifier efficiency. The waveforms at the intrinsic drain of the transistor correspond to time-reversed class-F waveforms. The gate-port load-pull contours are displayed in Fig. 4. The figure also shows the optimal impedance for  $\eta_R$  at f<sub>RF</sub> which is related to a dynamic load-line with a minimal enclosed area, and close to the I-V characteristic given at constant V<sub>gs</sub>.

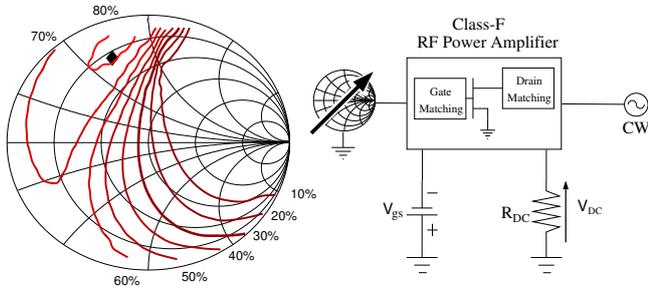


**Fig. 2** Simulated GaN transistor I-V curves (gray), dynamic load lines (red) and drain DC voltage and current (black) for the PA (a) and rectifier (b). The blue line is the V<sub>gs</sub> = -4.9V transistor characteristic (the gate bias point value is the same for both cases). Time-reversal duality is seen as the RF power at the drain is swept from 0 to 40 dBm at 2.14 GHz. The PA case has a drain bias of 28 V.



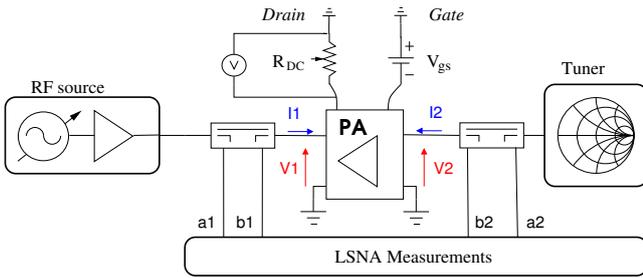
**Fig. 3** Simulated time-domain intrinsic drain voltage (blue) and current (red) waveforms for varying RF power at the drain in the case of a PA (a) and rectifier (b). In the case of the PA, V<sub>ds</sub> = 28 V.

**Measurements of PA and rectifier:** Measurements are performed on a single-transistor GaN class-F<sup>-1</sup> power amplifier detailed in [3]. This hybrid PA uses a TriQuint TGF2023-02 12-W bare die, and gives P<sub>out,RF</sub> = 7 W with over 84.6% PAE at a drain voltage of 31 V and with a 19 dB gain at 2.14 GHz. The output matching circuit is designed by load-pull and has terminated second and third harmonics which are designed to give class-F<sup>-1</sup> waveforms at the virtual drain reference plane. The gate is matched for large-signal gain at 2.14 GHz. This PA, biased at V<sub>gs</sub> = -4.4 V, was characterized in rectifier mode, with the reference plane set at the coaxial drain-port connector. A time-domain load-pull setup (Fig. 5) was used to obtain load-pull results at R<sub>DC</sub> = 98Ω shown in Fig. 6. The

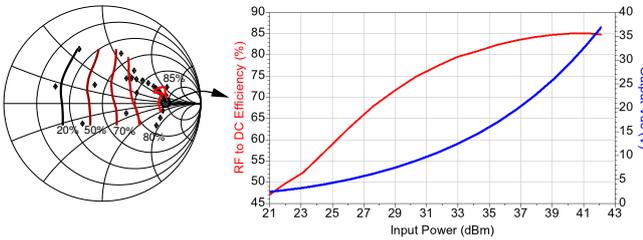


**Fig. 4** Load-pull simulations for rectifier efficiency obtained at the transistor terminals. The frequency is 2.45 GHz and RF drain input power is 40 dBm. The diamond symbol shows the impedance for maximal efficiency.

best rectifier efficiency  $\eta_R = 85\%$  is obtained for  $Z_{load} = (229 + j.9)\Omega$  at  $P_{in,RF} = 41$  dBm with  $V_{DC} = 31$  V.



**Fig. 5** Rectifier load-pull measurement setup. An RF power sweep is performed at the input drain port for each RF impedance provided by the tuner at the gate port. The output DC power delivered to the load  $R_{DC}$  is calculated from the DC voltage as measured by a voltmeter.



**Fig. 6** Rectifier performance measured at the coaxial reference planes ( $f_{RF} = 2.14$  GHz). Left: RF load impedances used for measurements (black dots), where the contours correspond to  $\max\{\eta_R\}$  for the complete power sweep applied to the RF drain port. Right:  $V_{DC}$  and  $\eta_R$  measured for  $R_{DC} = 98\Omega$  and  $Z_{load} = (229 + j.9)\Omega$

**Discussion:** While it was previously shown that harmonic terminations defined for power amplifier modes of operation can be used for diode and transistor rectifiers [4], the non-linear simulations and experiments in this letter demonstrate the time-reversal duality of high-efficiency microwave power amplifiers and rectifiers. In this case, the rectifier is obtained by operating the power amplifier in reverse mode, and the insight into transistor intrinsic waveforms is made possible by a GaN HEMT nonlinear model originally developed for switches. Over 80% conversion efficiency is demonstrated for both modes of circuit operation, starting from a harmonically-terminated PA design.

Note that the simulations and measurements for the rectifier are performed in self-synchronous mode, i.e. there is no input RF power incident externally into the gate port of the PA, unlike in previous lower-frequency transistor rectifier work [5][6]. This is possible due to the non-negligible nonlinear feedback capacitance  $C_{gd}$ , which couples some of the input RF signal from the drain to the gate. In the class-F simulations, an isolation of 18 dB is observed between the drain and the gate ports with  $C_{gd} \approx 108$  fF. With the appropriate gate complex impedance the transistor can operate as a self-synchronous rectifier.

**Acknowledgment:** This work was funded in part by the Office of Naval Research under the DARPA Microscale Power Conversion (MPC) Program under Grant N00014-11-1-0931, and in part by the Advanced Research Projects Agency- Energy (ARPA-E) under Award Number DE-AR0000216.

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